

# Dr.Roopa Nayak

## **Associate Professor and HOD, EEE Department**

### **Experience (Teaching 13 years 6 months)**

RNSIT (2003-Till date)

#### Qualifications

- B.E. from Manipal Institute of Technology
- M.Tech from JSS Academy of Technical Education
- Ph. D from VTU

#### **Specialization (Academics)**

- Analog Electronic Circuits
- Op-Amp and Linear Integrated Circuits
- Digital System Design
- Fundamentals of VLSI Design
- Power System Protection

#### **Specialization (Research)**

• Electric Drives

#### **Publications**

- Roopa Nayak, Shriraj, Chandan Gowda S, Arun Kumar S R, Ajay D, "Novel Methodology For Solar Panel Efficiency Enhancement", International Journal of Innovative Research in Technology, vol.11, issue 11, April 2025.
- Roopa Nayak, Dr. Andhe Pallavi, "Multi-Motor Octagonal Blender Drive", International Journal of Advanced Science and Technology, vol. 29 No. 05 (2020), pp. 6336-6345.
- Roopa Nayak, Andhe Pallavi, "Cost Analysis Based Algorithm for Load Shared Multiple Induction Motor Set-up", International Journal of Recent Technology and Engineering (IJRTE) ISSN: 2277-3878, vol. 8, issue-4, pp. 478-482, November 2019. DOI:10.35940/ijrte.D7100.118419
- Roopa Nayak, Andhe Pallavi, "A Comparison of V/f and Field Oriented Control of Three Phase Induction Motors Employed in Load Sharing" International Journal of Computer Sciences and Engineering, vol. 7, issue-13, pp. 49-56, May-2019. DOI: <a href="https://doi.org/10.26438/ijcse/v7si13.4956">https://doi.org/10.26438/ijcse/v7si13.4956</a>
- Roopa Nayak, Andhe Pallavi, "Novel V/f Strategy Using Command Speed Compensator for Improved Load Sharing with Dual Induction Motor", IJISET, vol.3, issue 2, February, 2016.

#### **Book Chapter**

Roopa Nayak, Andhe Pallavi, "Cost Analysis Based Strategy for Load Balancing in Multi-Induction Motor Systems", Chapter-1, pp.1-14, Engineering Research: Perspectives on Recent Advances, vo.4, 2025.



## **Patents**

Patents Published - 2

## Certifications

Data Science for Engineers, NPTEL

System Design through Verilog, NPTEL